Digital ASIC Fabrication

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Client: ***Dr. Henry Duwe***

Problem Statement:

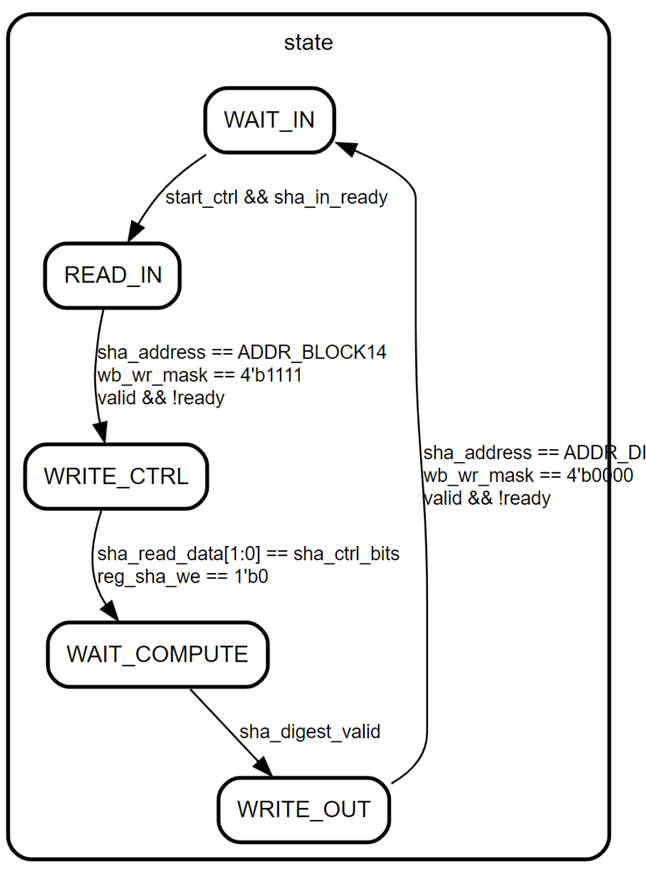
- Develop a process to fabricate digital ASICs through the MPW Shuttle program
- Create a bring-up plan for chip fabrications
- Design a SHA1 hashing accelerator for the MPW shuttle submission

Intended Use Cases:

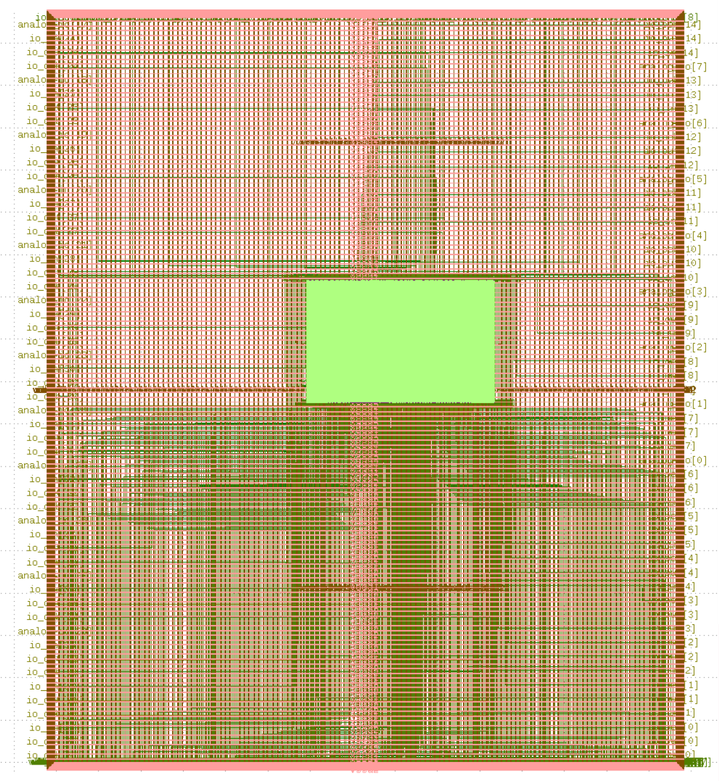
- Provide undergraduate students at Iowa State with a means to fabricate ASICs
- Reinforce hands-on oriented research pedagogy for hardware design senior design teams

Design Approach:

- State Machine Design



- Full Hardened Layout of our Design



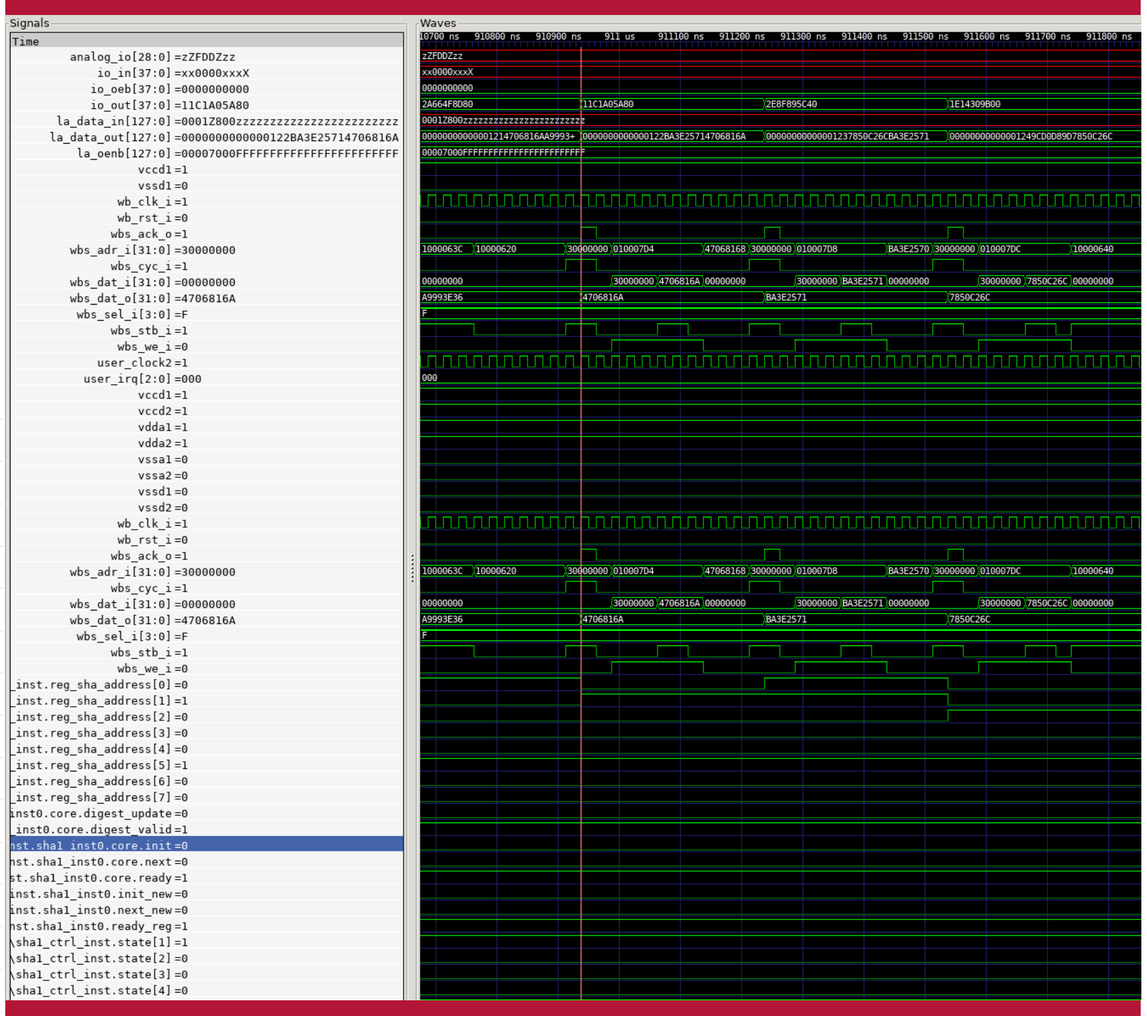
- Main security concern is the IP we brought in for the SHA 1 hash used in the design containing potentially malicious code. This is addressed by combing through files and testing of module to ensure no risk to our design.

Technical Details:

- Used Windows Subsystem for Linux (WSL) for Caravel User environment
- Created Verilog testbenches to test functional units
- Created firmware test cases in C running on SoC
- Probed signals using logic analyzer subcomponent
- Utilized Verilog within Efabless framework to implement our design

Testing:

- Multiple testbenches with various inputs like ‘abc’
- Correct output on ‘wbs_dat_o’
- Simulations passed RTL and GL tests
- Consisted of C & Verilog code
- Logic analyzer ports used as probes to ensure data in/out are correct
- eFabless submission process for precheck and tapeout
- Multiple trials of hardening so design physically fits & functions in user project area



Design Requirements:

- Design passes MPW precheck and tapeout
- RTL and GL chip simulation testbenches pass
- Design functions as a hardware accelerated SHA1 hasher (modified from Bitcoin miner)
- Simulate unit tests in the caravel simulation environment
- Design hardens through OpenLANE
- Power/timing constraints are met after hardening design
- The IP integrated has no security risk
- IEEE Standard VITAL ASIC (Application Specific Integrated Circuit) Modeling Specification - Designed an ASIC using a modeling standard allow us to clearly communicate our design to other engineers.
- IEEE Standard for Integrated Circuit (IC) Open Library Architecture (OLA)- Useful as it covers ways for integrated circuit designers to analyze chip timing & power consistently across a broad set of electric design automation (EDA) applications.

Project Resources:

- **Budget – $0**
- Manpower - A lot

Conclusion:

- All tests & requirements pass
- Submitted to eFabless
- Ready for manufacturing