sddec22-17: ASIC Fabrication

Week 1 Report
January 25 - February 6

Team Members

Soma Szabo — *Researcher (Tenative)*
Constantine Mantas — *Researcher (Tenative)*
Dawood Ghauri — *Researcher (Tenative)*
Courtney Violett — *Researcher (Tenative)*

Summary of Progress this Report

In this beginning report period, the overall objective was to get familiarized with the efabless process for designing and fabricating ASICs. Majority of the work spent was exploring the information presented on the website, the relevant tools that we have available to us, and communicating with our client (Dr. Duwe) on his expectations for us in this project along with the end outcome/goal. One of the more important parts moving forward in developing this project will be laying down a strong foundation for our workflow along with understanding what application our integrated circuit design will be implementing.

Pending Issues

As we are in the beginning stages of our project, these current issues are applicable to all team members.
- Researching Hardening and other pre-check requirements to be able to submit the project to Efabless.
- Emailing efabless about future shuttle runs and what those time tables will look like.
- Cloning Caravel user project to our GIT repository.
- Researching IP and other licenses we will need to complete the project.

Plans for Upcoming Reporting Period

Answer the following questions:
- What is on the chip fabrication PCB?
- How many PCBs do we get back?
- What is the minimum "novelty" for submission acceptance?
- How does the efabless process work and what tools are available?

Complete these tasks (tentative - will be updated):
- Clone caraval_user_project to public git repository (this is required for the efabless verification process).
- Run through the verification and testing process with the given caravel example project.
- Understanding the user_project_wrapper and how it connects with the main application.
- Using OpenLane to harden the design.

Individual Contributions

Team Member	Contribution	Weekly Hours	Total Hours
Soma Szabo	Researched the efabless tools and explored the Open MPW shuttle project for chip design	7	0

	requirements/options. Attended seminar for OpenMPW project and looked into potential IPs we could use for designing our chip.		
Constantine Mantas	Explored Efabless website and tools. Get a high-level understanding of the shuttle process and requirements. Find out how our design can interact with the Caravel chip harness. Watch videos of shuttle run walkthrough by the efabless team.	7	0
Dawood Ghauri	Attended efabless seminar on introductions to OpenMPW. Take a look at high-level implementations. Explored docker container requirements along with tools specific for efabless. Setting up personal workflow for project.	7	0
Courtney Violett	Explored requirements for using efabless prechecks verifying correctness. Watching the shuttle run webinar that was recently published by Efabless. Found basic example of a complete Caravel User project that explored the process of submitting a chip along with the example code of that basic project and reviewed it.	7	0

Gitlab Activity Summary

Nothing to report.