Senior Design Weekly Status Report

sddec22-17: ASIC Fabrication

Report 2

Feb 7, 2022 - Feb 13, 2022

Team Members:

Soma Szabo - Researcher / Component Design

Constantine Mantas - Researcher / Team organization leader

Dawood Ghauri - Researcher / Design Workflow

Courtney Violett - Researcher / Testing

Progress Summary:

The main objective this week was to fully understand the efabless MPW5 project and start experimenting with the caravel user project - the template for our custom ASIC design. This template was cloned, pushed to our own GitHub repository, and we began looking into the user project wrapper for ideas about what we can modify and include in our design. The local environment was also set up, but had issues running all Makefiles. A presentation was created to summarize all aspects of the design and how our user project will interface with the management SoC. The next milestone will be deciding what custom ASIC we want to implement in the user area of the chip. Additionally, we must fully understand the communication protocols and signals available between our custom design and the management SoC.

Past week accomplishments:

Soma Szabo - Worked on setting up the public GitHub repository, experimenting the caravel user project, and setting/understanding up the local environment. Investigated the hardware design and the layout for our chip implementation.

Dawood Ghauri - Working alongside Soma to run through the initial round trip document (published by eFabless) which assists in proper setup of the local environment and GitHub. Passing most of the parts for the given example caravel user project and wrapper, but pending on finalizing pre-check.

Constantine Mantas - Set up a process presentation and begin adding information as well as relevant images. Emailed efabless with questions about future shuttle runs. Worked on building a local environment for the caravel user project.

Courtney Violett - Worked on better understanding the process of chip hardening and explored some of the different options about the hardening process. Helped contribute to the process presentation specifically on elaborating on the hardening process.

Pending Issues:

- Webinar on verifications and analysis on Wednesday 9am. Also check to see if a video of it is posted to the Efabless youtube channel. (Courtney and Dawood will attempt to be there on Wednesday. All will watch if posted online)
- Find out about, logic analyzer, interrupt signal. (Courtney)
- Find out how big the memory is. (Constantine)
- Find out what type of power control we have. Find out if we can run at a variable clock rate. (Soma)
- Find out what type of design we want to work on. (All)
- Finding out how the wishbone connection works between the user space and management SOC and what sort of communication can be done across it. (Dawood)
- Finalize going through setting up the local environment and going through pre-check for given example (ALL).

Individual Contributions:

https://docs.google.com/spreadsheets/d/16JZdcN7ZWrpaEueMXxc_UKMeUQITxlRqzQzuwnaxndY/edit?usp=sharing

Summary of weekly advisor meeting (if applicable/optional):

We presented a rough draft presentation of current research findings on efabless design process and technology available to use in chip design as well as discussion on what to focus on in the upcoming week.

Business and Technology Methodologies (Competitor Benchmarking):

	Donkey Kong Drums	TDC Converter	Multiplication Division Unit
Novelty	3	1	1
Innovation	2	2	2
Technologically Adv.	1	2	2
Global Presence	1	3	1

Low: 1

Medium: 2

High: 3