Senior Design Weekly Status Report

sddec22-17: ASIC Fabrication

Report 3

Feb 14, 2022 - Feb 20, 2022

Team Members:

Soma Szabo - Researcher / Component Design

Constantine Mantas - Researcher / Team organization leader

Dawood Ghauri - Researcher / Design Workflow

Courtney Violett - Researcher / Testing

Progress Summary:

The main objective this week was to finalize the *roundtrip* test run for the given example project and begin thinking about the application our ASIC will be running. A few issues still remain in the *roundtrip* finalization (which involves the setup of our local environments to run the eFabless software), but we're almost complete with this task. We discussed with our client about further familiarizing ourselves with the hardware ports, conventions, and limitations prior to application integration, and we came up with an idea to first implement a basic adder (from our collective knowledge in taking CPRE 381) in the user project workspace. This will allow us to get a deeper understanding of the open source tools eFabless is employing in its workflow so we can move forward with our application idea: A Bitcoin Hashing Accelerator. Further discussion on the background and methodology used to implement this idea will be presented in a future report, but we are in unanimous agreement to move forward in this direction.

Past week accomplishments:

Soma Szabo - Looked into the Bitcoin mining application for the chip design project, started exploring the hardware needed to implement it, experimented with building the local design environment, and got ready to simulate the design with custom HDL to better understand integration capabilities.

Dawood Ghauri - Further debugged the local workspace to pass the *make run-precheck* part of the *roundtrip* documentation. This is the last step to complete setup of the workspace, but an issue remains with a "GOLDEN_CARAVEL" variable that is still unresolved. Researched the bitcoin mining application at a high-level presented in a paper co-authored by Dr. Duwe. Researched the wishbone connection framework and found that it operates under a master/slave paradigm. That is, it has ports similar to the AXI Stream related to data validation and uses a handshake to pass data between the user project space and the RISC-V processor in the management area of the caravel harness.

Constantine Mantas - Worked on setting up the workspace enabled to interface with the caravel harness. Researched potential chip designs. Researched hardware limitations of caravel harness.

Courtney Violett - Worked on understanding the Logic analyzer in the management SoC. Found examples of the LA(logic analyzer) being used for interrupts and other data verification from the Project management area. Also found an example of an irq based on data from the user project area.

Pending Issues:

- Build and test a simple adder circuit in the caravel work environment.
- High level schematic of the design.
    - The adder and the bitcoin ming core.
- Finalize going through setting up the local environment and going through pre-check for given example (ALL).
- Look into Open Cloud (VM) and using git to share the workspace and tools
- Potentially explore bring-up processes for chips (such an UVM)

Individual Contributions:

https://docs.google.com/spreadsheets/d/16JZdcN7ZWrpaEueMXxc_UKMeUQITxlRqzQzuwnaxndY/edit?usp=sharing

Summary of weekly advisor meeting (if applicable/optional):

A concise summary on the contents and progress made during the advisor meeting.

Discussed the hardware limitations based on our research and used that information to decide on a chip design idea we may submit for the shuttle. The current goal is to ensure a Bitcoin mining core can fit on the provided chip and can run the necessary firmware to execute the cryptocurrency mining process. After making this decision, we talked about the next steps for the project as well as potential future roadblocks regarding this design choice.