Senior Design Weekly Status Report

sddec22-17: ASIC Fabrication

Report 5

Feb 28, 2022 - Mar 6, 2022

Team Members:

Soma Szabo - Researcher / Component Design

Constantine Mantas - Researcher / Team Organization Leader

Dawood Ghauri - Researcher / Design Workflow

Courtney Violett - Researcher / Testing

Progress Summary:

The main objective this week was to get a simple adder implementation setup inside the caravel user project. The idea behind getting this setup is for the team to get more familiarized with how to create modules within the caravel user project which will then connect with the wrapper. By doing this, we are also getting more familiar with the logic analyzer, wishbone connections, and I/O pads. Our immediate next step is to get a testbench setup for the adder to better understand the testing process for custom implementations. Additionally, with the caravel user project release of ***mpw-5c***, we were able to get the local development environment setup for all users as this included a lot of bug fixes.

Past week accomplishments:

Soma Szabo - The local design environment was set up and created a new official repository for the Bitcoin ASIC hardware design based on the mpw5-c release. An adder was created in the wrapper design and started testing it. The specifications for the caravel project are being further explored to be able to create a high level design for the Bitcoin ASIC.

Dawood Ghauri - Created a trivial adder/subtractor verilog module (still pending testing). Further researched the logic analyzer (using it as a dedicated clock and reset) and the wishbone connection ports (how it will be sending data streams to the adder/subtractor – similar to AXI Stream protocol).

Constantine Mantas - Finished setting up the workspace enabled to interface with the caravel harness. Also watched/researched a verification presentation from Efabless about their process for verifying Caravel User project submissions.

Courtney Violett - Finished setting up the work environment for developing within Efabless and specifically our project with the caravel harness. Also watched/researched a verification presentation from Efabless about their process for verifying Caravel User project submissions.

Pending Issues:

- Test our simple adder circuit in the caravel work environment.
- More detailed schematic of the hardware design.
    - The adder and the bitcoin ming core.
- Look into Open Cloud (VM) and using git to share the workspace and tools
- Potentially explore bring-up processes for chips (such an UVM)
- Finish instructions for future users on setting up the dev environment for both Windows and Mac.
- Look up how they are doing their testing verification for the testbenches

Individual Contributions:

2/28/2022 - 3/6/2022	
Individual Contributions (short)	**Weekly Hours**
Set up the local design environment, created a new official repository for the Bitcoin ASIC hardware design. An adder module was created in the wrapper design and started testing it. Looking into the Caravel project specifications for more information.	6
Finished setting up the workspace enabled to interface with the caravel harness. Also watched/researched a verification presentation from Efabless about their process for verifying Caravel User project submissions.	6
Created a trivial adder/subtractor verilog module (still pending testing). Further researched the logic analyzer (using it as a dedicated clock and reset) and the wishbone connection ports (how it will be sending data streams to the adder/subtractor – similar to AXI Stream protocol).	6
Finished setting up work environment, and watched/ researched Efabless's verification process of Caravel Projects.	6

Summary of weekly advisor meeting (if applicable/optional):

A concise summary on the contents and progress made during the advisor meeting.

Our meeting this week started with talking about our current progress and how we should move forward to properly test the adder we built. Then the conversation shifted towards future planning for how we will modularly build our bitcoin mining circuit and have a proper testing plan for it.