Senior Design Weekly Status Report

sddec22-17: ASIC Fabrication

Report 6

Mar 7, 2022 - Mar 13, 2022

Team Members:

Soma Szabo - Researcher / Component Design

Constantine Mantas - Researcher / Team Organization Leader

Dawood Ghauri - Researcher / Design Workflow

Courtney Violett - Researcher / Testing

Progress Summary:

The main objective this week was to get an automated testing framework for a simple adder that we designed and to experiment with the efabless testing process to get a better understanding of how our design interacts with the Management SOC. We managed to make good progress and confirm the functionality of the adder through testing, however we still need to be able to automatically recognize proper output using the logic analyzer for the testing to be fully automated.

Past week accomplishments:

Soma Szabo - The largest accomplishment was getting the adder implementation to work and simulating it (the entire chip) in the local test environment. In addition to finalizing the adder and creating the test bench for it, the overall chip design was further researched and the hardware/firmware integration was better understood. This will allow for more complex designs in the future.

Dawood Ghauri - Worked on researching how the testing framework of Efabless' Open MPW shuttle example works, and helping to implement similar testing measures in our own adder design.

Constantine Mantas - Worked on researching how the testing framework of Efabless' Open MPW shuttle example works, and helping to implement similar testing measures in our own adder design.

Courtney Violett - Switched over to mpw-5. Researched the verification that Efabless does when testing and verifying that a submitted project will work properly. Looked over the test cases and adder that Soma and Dawood put together to become familiar with the testing processes and making components for our project.

Pending Issues:

- Perform more complex tests on the adder circuit in the caravel work environment.
- More detailed schematic of the hardware design.
    - The adder and the bitcoin ming core.
- Look into Open Cloud (VM) and using git to share the workspace and tools
- Potentially explore bring-up processes for chips (such an UVM)
- Finish instructions for future users on setting up the dev environment for both Windows and Mac.
- Look up how they are doing their testing verification for the testbenches
- Look into sha-256 IP
- Look into creating different kinds of adders and testing them.

Individual Contributions:

3/7/2022 - 3/13/2022		
Name	**Individual Contributions (short)**	**Weekly Hours**
Soma Szabo	Finalized the adder and the testbench for it. Simulated the design and researched the caravel project to allow for more complex designs in the future. The hardware/firmware integration was better understood	6
Constantine Mantas	Worked on researching how the testing framework of Efabless' Open MPW shuttle example works, and helping to implement similar testing measures in our own adder design.	6
Dawood Ghauri	Worked on researching how the testing framework of Efabless' Open MPW shuttle example works, and helping to implement similar testing measures in our own adder design.	6
Courtney Violett	Switched over to mpw-5. Researched the verification that Efabless does when testing and verifying that a submitted project will work properly. Looked over the test cases and adder that Soma and Dawood put together to become familiar with the testing processes and making components for our project.	6

Summary of weekly advisor meeting (if applicable/optional):

A concise summary on the contents and progress made during the advisor meeting.

Senior Design Weekly Status Report

Our meeting this week started with talking about our current progress and how we should move forward to finish testing the adder we built. Then the conversation shifted towards future planning for how we will plan and design the rest of our bitcoin mining ASIC.