Senior Design Weekly Status Report

sddec22-17: ASIC Fabrication

Report 7

Mar 21, 2022 - Mar 27, 2022

Team Members:

Soma Szabo - Researcher / Component Design

Constantine Mantas - Researcher / Team Organization Leader

Dawood Ghauri - Researcher / Design Workflow

Courtney Violett - Researcher / Testing

Progress Summary:

The main objective of this week was to continue development of our general purpose adder along with its testing. We have achieved proper operation by considering three different tests, but are still in the process of getting communication from the slave (user side) to the master (SoC side) through the wishbone to where the testing framework resides (to validate testing). In addition, we developed a state machine which emulates the nonce incrementation process which will be the primary purpose of our adders. The main next steps are continuing work on communication through the wishbone and also choosing an IP to implement the core functionality of the hash function in hardware.

Past week accomplishments:

Soma Szabo - The adder and the test bench for it was modified and the wishbone bus protocol was further understood. This allows for a previous result input to the adder and can use that in computation if desired. The logic analyzer signals were also understood and gained a better overview of the design for our Bitcoin mining ASIC.

Dawood Ghauri - Worked on testing for the adder and also configuring the workflow for the local environment. The logic analyzer is a key component that Soma and I used for these tests as it gives more direct control over states needed.

Constantine Mantas - Worked on researching how the testing framework of Efabless' Open MPW shuttle example works, and helping to implement similar testing measures in our own adder design.

Courtney Violett - Researched the verification that Efabless does when testing and verifying that a submitted project will work properly. Looked over the test cases and adder that Soma and Dawood put together to become familiar with the testing processes and making components for our project.

Pending Issues:

- Finish complex tests on the adder circuit in the caravel work environment.
- More detailed schematic of the hardware design.
    - The adder and the bitcoin ming core.
- Look into Open Cloud (VM) and using git to share the workspace and tools
- Potentially explore bring-up processes for chips (such an UVM)
- Finish instructions for future users on setting up the dev environment for both Windows and Mac.
- Look up how they are doing their testing verification for the testbenches
- Look into sha-256 IP
- Look into creating different kinds of adders and testing them.

Individual Contributions:

3/21/2022 - 3/27/2022		
Name	**Individual Contributions (short)**	**Weekly Hours**
Soma Szabo	The adder and the test bench for it was modified and the wishbone bus protocol was further understood. This allows for a previous result input to the adder and can use that in computation if desired. The logic analyzer signals were also understood and gained a better overview of the design for our Bitcoin mining ASIC.	7
Constantine Mantas	Worked on researching how the testing framework of Efabless' Open MPW shuttle example works, and helping to implement similar testing measures in our own adder design.	6
Dawood Ghauri	Worked on testing for the adder and also configuring the workflow for the local environment. The logic analyzer is a key component that Soma and I used for these tests as it gives more direct control over states needed.	5
Courtney Violett	Researched the verification that Efabless does when testing and verifying that a submitted project will work properly. Looked over the test cases and adder that Soma and Dawood put together to become familiar with the testing processes and making components for our project.	5

Summary of weekly advisor meeting (if applicable/optional):

A concise summary on the contents and progress made during the advisor meeting.

The meeting revolved around understanding the wishbone communication protocol and discussing the waveforms of our test benches. We also discussed the high level design and future plans for the Bitcoin mining ASIC so we have a better understanding of the direction to move forward in. This will be researching a SHA-256 hardware IP module and trying to integrate a simple state machine for controlling it.