Senior Design Weekly Status Report

sddec22-17: ASIC Fabrication

Report 8

Mar 28, 2022 - Apr 2, 2022

Team Members:

Soma Szabo - Researcher / Component Design

Constantine Mantas - Researcher / Team Organization Leader

Dawood Ghauri - Researcher / Design Workflow

Courtney Violett - Researcher / Testing

Progress Summary:

This week we finished testing a simple adder and accumulator unit that takes input through the wishbone and sends it back through it as well. It can also use the previous result, along with a custom number through the wishbone, allowing for 32-bit addition/subtraction (instead of two 16-bit). Our unit test for it now passes and we are getting expected values from the adder and are able to read and write over the wishbone port. We also have found a couple potential IPs to use in our ASIC design. The IPs will need to be validated and we still need to determine how we will be integrating one of them into the user space on the caravel harness. We have our design plan in an executable state now and any changes to it further will be from changes that need to be made during the implementation of it.

Past week accomplishments:

Soma Szabo - The adder was finished in the user project area of the SoC and more complex test benches were added. The adder has a feature for using the previous result as input/output through the wishbone and can accumulate or do computations with the previous result. The I/O and

debug ports for the user space are now well understood and can start planning the Bitcoin ASIC design while considering any requirements/constraints we may have such as SRAM or logic analyzer (debug ports).

Dawood Ghauri - Worked on the design plan and test plans for our project. After meeting with our client, it is clear to us that a well-laid out test plan will be a major part of our project. Therefore, additional development in the future is needed so that our test plan is comprehensive. Looked into OpenRAM briefly; may serve as a memory macro if we are unable to access fast memory close to our project area on the chip.

Constantine Mantas - Worked on a design plan and a rough test plan for our project.

Courtney Violett - Helped with the design plan. Also worked on finding potential SHA-256 IP that we can use on our design. Began to work on a test plan for our project as well.

Pending Issues:

- Attempt to integrate the SHA-256 IP we found
    - Look into what other design aspects may go into getting the hasher to function
- More detailed schematic of the hardware design.
    - The adder and the bitcoin ming core.
- Find the best method to perform design verification with testbenches
- Create detailed figure to illustrate test plan
- Give a more detailed high level overview of the test plan
- Find a reliable way to verify the SHA-256 module output
- Look into creating different kinds of adders, test them, and integrate them into the SHA-256 module.

Individual Contributions:

3/28/2022 - 4/2/2022		
Name	**Individual Contributions (short)**	**Weekly Hours**
Soma Szabo	The adder was finished, with additional features implemented, and more complex test benches were created. The I/O and debug ports for the user space are now well understood and can start planning the Bitcoin ASIC design while considering any requirements/constraints we may have such as SRAM or logic analyzer (debug ports).	6
Constantine Mantas	Worked on a design plan and a rough test plan for our project.	6
Dawood Ghauri	Worked on design plan and test plan for our project; next steps to iterate on testing plan as it will be a major component of our project. Additionally, researched briefly into OpenRAM which could potentially serve as a memory macro should we be unable to find on chip memory which is fast enough for our needs.	6
Courtney Violett	Helped with the design plan. Also worked on finding potential SHA-256 IP that we can use on our design. Began to work on a test plan for our project as well.	6

Summary of weekly advisor meeting (if applicable/optional):

A concise summary on the contents and progress made during the advisor meeting.

The meeting revolved around presenting our current design and test plan to our client/advisor and receiving feedback on how to improve them. We also discussed our current goals for this semester should be and what our next steps to achieve those goals will be.